What is claimed is:

1. A dual-bit nitride read only memory cell with parasitic amplifier, comprising:

a semiconductor substrate;

a first well region disposed in the semiconductor substrate and having a first conductive type opposite to the semiconductor substrate;

a second well region disposed in the first well region and having a second conductive type opposite to the first well region;

a gate dielectric layer disposed over portions of the second well region, wherein the gate dielectric layer comprises a nitride layer;

a conductive layer disposed on the gate dielectric layer to form a gate; and

a pair of first doped regions symmetrically disposed in the second well region on both sides of the gate and having a third conductive type opposite to the second well region, wherein one of the first doped regions, the second well region and the first well region constitute a parasitic current amplifier.

2. The nitride read only memory cell as claimed in claim 1, wherein the semiconductor substrate is a P-type silicon substrate.

3. The nitride read only memory cell as claimed in claim 1, wherein the conductive layer is comprised of polysilicon.

4. The nitride read only memory cell as claimed in claim 1, wherein the first doped regions are N-type doped regions having a doping concentration between $1*10^{19}$ and $1*10^{21}$ atoms/cm^2.

5. The nitride read only memory cell as claimed in claim 1, further comprising a pair of second doped regions symmetrically disposed in the first well region on both sides of the gate.

6. The nitride read only memory cell as claimed in claim 5, wherein the second doped regions are N-type doped regions having a doping concentration between $1*10^{19}$ and $1*10^{21}$ atoms/cm^2.

7. The nitride read only memory cell as claimed in claim 1, wherein the parasitic current amplifier is a bipolar junction transistor (BJT) including an emitter constituted of one of the first doped regions, a base constituted of the second well region and a collector constituted of the first well region.

8. The nitride read only memory cell as claimed in claim 1, wherein the gate dielectric layer is oxide-nitride-oxide (ONO) layer.

9. A method of fabricating a dual-bit nitride read only memory cell, comprising the steps of:

providing a semiconductor substrate;

forming a first well region in the semiconductor substrate, and the first well region having a

first conductive type opposite to the semiconductor substrate;

forming a second well region in the first well region, and the second well region having a second conductive type opposite to the first well region;

sequentially forming a dielectric layer and a conductive layer over the second well region to form a gate thereon, wherein the dielectric layer comprises a nitride layer; and

symmetrically forming a pair of first doped regions in the second well region on both sides of the gate, and the first doped regions having a third conductive type opposite to the second well region, wherein one of the first doped regions, the second well region and the first well region constitute a parasitic current amplifier.

10. The method as claimed in claim 9, wherein the dielectric layer is an oxide-nitride-oxide layer.

11. The method as claimed in claim 9, wherein the first doped regions are N-type doped regions having a doping concentration between $1*10^{19}$ and $1*10^{21}$ atoms/cm^2.

12. The method as claimed in claim 9, further comprising the step of symmetrically forming a pair of second doped regions in the first well region on both sides of the gate.

13. The method as claimed in claim 12, wherein the second doped regions are N-type doped regions having a doping concentration between $1*10^{19}$ and $1*10^{21}$ atoms/cm^2.

14. The method as claimed in claim 9, wherein the semiconductor substrate is a P-type silicon substrate.

15. The method as claimed in claim 9, wherein the conductive layer is comprised of polysilicon.

16. The method as claimed in claim 9, wherein the parasitic amplifier is a bipolar junction transistor (BJT) including an emitter constituted of one of the first doped regions, a base constituted of the second well region and a collector constituted of the first well region.

17. A method of reading a dual-bit nitride read only memory cell constituted of a semiconductor substrate, a first well region having a first conductive type opposite to the substrate disposed in the substrate, a second well region having a second conductive type opposite to the first well region disposed in the first well region, a gate dielectric layer comprising a nitride layer disposed over portions of the second well region, a conductive layer disposed on the gate dielectric layer to form a gate, and a pair of first doped regions symmetrically having a third conductive type opposite to the second well region disposed in the second well region on both sides of the gate, wherein one of the first doped regions, the second well region and the first well region

constitutes a parasitic current amplifier, comprising the steps of:

selecting a reading bit of the dual-bit nitride read only memory cell, floating the gate and grounding one of the first doped region on the opposite side thereof;

applying a first voltage to the other first doped region adjacent to the reading bit to generate a leakage current into the second well region;

applying a second voltage to the first well region on the opposite side of the reading bit to turn on the current amplifier therein and amplify the leakage currents; and

measuring an amplified current from the first well region on the opposite side of the reading bit to acquire the memory status of the reading bit.

18. The method as claimed in claim 17, wherein the reading bit is 0 when the amplified current is less than 10^{-2} μA.

19. The method as claimed in claim 17, wherein the reading bit is 1 when the amplified current exceeds or equal to 10^{-2} μA.

20. The method as claimed in claim 17, wherein the first voltage is between 1 and 10 volts.

21. The method as claimed in claim 17, wherein the second voltage is between 1 and 10 volts.

22. The method as claimed in claim 17, wherein the parasitic current amplifier has a current gain about 1 fold to 100 folds.

23. The method as claimed in claim 17, wherein the leakage currents are gate-induced drain leakages (GIDL).

24. The method as claimed in claim 17, wherein the second voltage is applied to a second doped region in the first well region on the opposite side of the reading bit.

25. The method as claimed in claim 24, wherein the second doped region is N-type doped region having a doping concentration between $1*10^{19}$ and $1*10^{21}$ atoms/cm^2.